REMARKS

Applicants wish to thank the Examiner for the telephonic conversation. As discussed on the telephone, if the Examiner feels another phone call would be helpful at the time of reviewing this response, Applicants would be happy to work with the Examiner.

Claims 1-13, 15-21, and 23-27 will be pending in the current Application. Claims 1-3, 8-10, 18, 23, 24, 26, and 27 have been amended herein. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claim Rejections under 35 U.S.C. § 102

Claims 1-9, 13-17, and 21-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,604,877 to Hoyt et al. (hereinafter "Hoyt"). Claims 10-12 and 18-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,205,536 to Toyohiko Yoshida (hereinafter "Yoshida"). Applicants respectfully traverse the rejections.

Claims 1, 3, and 24 and their Dependent Claims

Claims 1, 3, and 24 each include generating a first sequence signal that when negated indicates that the first address may not be sequential to the second address, a second sequence signal that when negated indicates that the first address is not sequential to the second address, and a third sequence signal that when negated indicates that the first address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the first address, if it is an instruction address, is sequential to the immediately preceding instruction address. Therefore, Applicants have replaced the use of "current" and "previous" with "first" and "second," respectively. In this manner, it is clear in each of claims 1, 3, and 24 that each of the first, second, and third sequence signals are asserted

with respect to a *same* first address. The Examiner, in the Response to Arguments, argued that the term "current" may be current with respect to position (being the next address) in addition to being with respect to time. However, note that the use of "first address" rather than "current address" makes it clear that all references are to a same first address, with respect to time, since the use of the "the" in front of each subsequent occurrence of "first address" in claims 1, 3, and 24 provides proper antecedent basis, thus indicating that it is referring back to the same "a first address" initially introduced in each claim. That is, unlike the "current" address which can indicate any address that is "current" in time, the first address is a fixed address with respect to time. Furthermore, Applicants have amended each of claims 1, 3, and 24 to clarify that the first address and the second address are provided on the address bus without any intervening addresses on the address bus. That is, there are physically no addresses provided on the address bus between the first and second addresses.

The Examiner, in the first interpretation, states that the first sequence signal is taught by the hit signal in Hoyt, the second sequence signal is taught by the prediction signal in Hoyt which indicates the predicted direction of the branch (i.e. whether the branch is predicted taken or not-taken), and the third sequence signal is the branch outcome signal of Hoyt. In a second interpretation, the Examiner states that the first sequence signal is taught by the hit signal in Hoyt, the second sequence signal taught by the branch outcome signal of Hoyt, and the third sequence signal taught by a signal which indicates whether the incremented PC address should be used or predicted branch target. Applicants respectfully submit that these interpretations are incorrect.

While the hit signal and the predicted direction may give information about the next address to be fetched (i.e. a "first" address) after the branch instruction (i.e. a "second" address), the branch outcome signal does not give information about that same first address. At the time the branch outcome signal is asserted or negated, the "first" address (the one immediately following the "second" address on the address bus) has long since passed. Therefore, in the Examiner's example, a branch is assumed at address 0000 which has a target address of 1111. The Examiner then states that the previous address (now second address, as claimed) is therefore 0000 and if the branch is predicted taken, the current address (now first address, as claimed) is 1111. The Examiner then proceeds to state "However, if a misprediction occurs shortly thereafter, then the current address is not 1111. Instead, the current address is 0001, as this is the

correct address to fetch from at this point in time. Note that in either case, both addresses (0001 and 1111) may be considered 'the current address' because both contain instructions which, based on the circumstance, are to be fetched immediately after fetching an instruction from the previous address." However, as stated above, Applicants have clarified claims 1, 3, and 24 by referring to the first address rather than a current address. Therefore, the first address cannot be both 0001 and 1111 because once the Examiner uses 1111 as the first address, 0001 cannot also be considered "the" first address.

Furthermore, the first address (0001) is not immediately following the second address (0000) on the address bus, as required in each of claims 1, 3, and 24. The Examiner states that "in the case where 0001 becomes the current address after an incorrect taken prediction, address 0001 is immediately following the previous address as far as fetching is concerned. Address 1111 was incorrect and therefore, the system is to act as if instruction were never fetched from that location and any subsequent location." However, this is incorrect. Although, in the case of a misprediction, the system is to "act as if instruction were never fetched from that location", the truth is, they were fetched (even though they were "wrongly fetched") and thus provided on the address bus. That is, in the Examiner's example, there are many intervening addresses provided on the address bus between 0000 (the time at which the wrong prediction was made) and 0001 (the time when the actual branch outcome was known). Therefore, 0001 cannot be the "first address" since it does not immediately follow 0000 on the address bus. Simply because the intervening addresses in Hoyt should be "ignored" does not mean they did not occur; that is, they are intervening addresses on the address bus, regardless of whether they are used or ignored. Therefore, note that the branch outcome signal of Hoyt does not provide any sequentiality information with respect to *the first address* (the next instruction to be fetched after the branch instruction or 1111 in the Examiner's example), as claimed in claims 1, 3, and 24.

Therefore, Hoyt does not teach or suggest the first, second, and third sequence signals as claimed in claims 1, 3, and 24, and for at least these above stated reasons, Applicants submit that claims 1, 3, and 24 are allowable over Hoyt. Claims 2, 4 - 9, 21 and 23 each depend, directly or indirectly, on claims 1 and 3 and therefore are allowable for at least the same reasons that claims 1 and 3 are allowable, as set forth above.

Claim 13 and its Dependent Claims

Claim 13 also stands rejected over Hoyt. Claims 13 includes providing a first sequence signal and a second sequence signal *for each address provided on the address bus*. The Examiner states that the first sequence signal is taught by the hit signal of Hoyt and that the second sequence signal is taught by the branch outcome. However, the hit and branch outcome signals are not provided for each address provided on the address bus, as claimed in claim 13. Even if the Examiner assumes that a hit/miss signal is provided with each address on the address bus (whether the address be for a branch or not) where this hit/miss signal could only be asserted when the address is for a branch instruction, a branch outcome signal indicating if the branch was predicted correctly or not is *not* provided for each address on the address bus, because it is only provided for branch instructions. For example, if a particular address is not for a branch instruction (hence, a BTB hit would not be asserted), a branch outcome signal would not be generated at all since there is no prediction made for that particular address. Therefore, Hoyt does not teach of suggest the first and second sequence signals of claim 13.

Claims 14 – 17, 22, and 25 each depend either directly or indirectly on claim 13 and, therefore, are allowable for at least the same reasons that claim 13 is allowable.

With respect to claim 25, claims 25 is also allowable for at least those reasons provided with respect to claim 13. Note that claims 13 also claims that that if the second sequence signal indicates that the address is not sequential to the immediately preceding address, the second sequence signal indicates that the address is not sequential to the immediately preceding address *in response to resolving a conditional branch.* Claim 25 further claims that if the second sequence signal indicates that an address is not sequential to the immediately preceding address, the first signal indicates that the address may not be sequential to the immediately preceding address in *a same clock cycle* as the second sequence signal indicating that the address is not sequential to the immediately preceding address. Note that the hit signal and branch outcome signal of Hoyt, which the Examiner stated teaches the first and second sequence signals of claim 13, do not occur in a same clock cycle. In rejecting claim 25, the Examiner refers to a signal which indicates whether to use the PC or a target address as teaching the second signal; however, this signal is not generated in response to resolving a conditional branch, as claimed in claim 13. Therefore, for these additional reasons, Applicants submit that claim 25 is allowable over Hoyt.

Claims 10 and 18 and their Dependent Claims

Claims 10 has been amended to further clarify that the first sequence signal is provided with the current address for use by the instruction memory. In addressing claim 26, which originally included this element, the Examiner cites figure 4.22 of Hennessy. However, this figure represents a branch target buffer, which is not the same as the claimed instruction memory. In order to clarify the instruction memory, Applicants have also amended claim 10 to clarify that the first instruction is stored at the first address in the instruction memory and the second instruction is stored at the second address in the instruction memory. Therefore, unlike the branch target buffer of Hennessy, the instruction memory of claim 10 returns the instructions stored at the instruction addresses provided on the address bus. However, the branch target buffer of Hennessy checks the PC (i.e. address) of an instruction to be fetched and if there is a hit, outputs another address (predicted PC for the target). That is, instructions are not provided from the branch target buffer of Hennessy. Therefore, this does not teach or suggest the instruction memory of claim 10, and furthermore, there is no teaching or suggestion in Hoyt or Hennessy to provide any branch prediction signal (the signal the Examiner uses as the first sequence signal in claim 10) out with the next fetch address for use by an instruction memory. That is, once the branch prediction is made, this signal is not longer needed for that address, and it would unnecessarily complicate the system of Yoshida to provide this irrelevant and no longer needed signal along with the next fetch address. Furthermore, there is no teaching, suggestion, or even motivation to also provide this previously generated branch prediction signal along with the current address for use by the instruction memory, as claimed in claim 10. Therefore, for at least these reasons, Applicants submit that claim 10 is patentable over Yoshida and Hennessy or their combination.

Applicants have also amended dependent claim 27, depending from claim 10, to further clarify that a data address is an address that stores data that is not an instruction, and does not simply indicate that the address itself can be considered data. Note that there is also no teaching or suggestion in Yoshida of negating the branch prediction signal during a data address. Therefore, for at least these additional reasons, Applicants submit that claim 27 is also allowable over Yoshida.

With respect to claim 18, Applicants have also amended claim 18 to include the instruction memory. That is, the instruction addresses are provided on the address bus to an instruction memory where the instruction memory has instructions stored at the instructions addresses. Furthermore, claim 18 includes providing the first sequence signal with the instruction address for use by the instruction memory. The Examiner states that the first sequence signal is "merely any signal which dictates that a prediction is or is not to be used...for instance, a first signal exists which would cause the system to either use a predicted address for a branch (which would be non-sequential) or to use an incremented value of the program counter." However, again, this signal (which dictates whether prediction is or is not to be used) must also be generated prior to providing the address (i.e. the address for which it provides sequentiality information) because this address has to be known before it can be fetched from. Furthermore, this previously generated signal is not then provided with the address it was used to generate. Once the current address is generated and provided in Yoshida, the signal which *was* used to indicate whether prediction was or was not to be used to generate this current address is no longer needed or even relevant to the current address. Therefore, there is no teaching, suggestion, or even motivation in Yoshida to also provide this previously generated signal (which, after generating the current address, is no longer needed or relevant to the current address) along with the current address itself and for use by an instruction memory. Therefore, for at least these reasons, Applicants submit that claim 18 is not taught or suggested by Yoshida or Hennessy or their combination.

Consequently, Yoshida fails as a 102 reference in that it does not teach each and every limitation claimed by Applicants. Therefore claims 10 and 18 are allowable over Yoshida. Claims 11, 12, 19 and 20 each depend, either directly or indirectly on claims 10 and 18 and, therefore, are allowable for at least the same reasons that claims 10 and 18 are allowable.

Conclusion

Applicants submit that the remaining claims in the Application are in condition for allowance and a Notice of Allowance is respectfully requested. If a discussion with Applicants' representative would be helpful in addressing any issues of patentability, Applicants respectfully request that the Examiner contact Applicants' attorney using the contact information provided below.

If Applicants have overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: _____

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